CLAIMS

We claim:

1. A method of designing an integrated circuit to improve yield when manufacturing the integrated circuit, the method comprising:

obtaining a design element from a set of design elements used in designing integrated circuits;

creating a variant design element based on the obtained design element, wherein a feature of the obtained design element is modified to create the variant design element;

determining a yield to area ratio for the variant design element; and

if the yield to area ratio of the variant design element is greater than a yield to area ratio of the obtained design element, retaining the variant design element to be used in designing the integrated circuit.

2. The method of claim 1, wherein the design element is a bit cell, the set of design elements is a set of bit cells, and the variant design element is a variant bit cell, and further comprising:

selecting a memory macro from a set of memory macros; and

applying the variant bit cell to the selected memory macro.

3. The method of claim 2, wherein the variant bit cell is applied to each of the memory macros in order of size from smallest memory macro to largest memory macro.

4. The method of claim 3, wherein determining a yield to area ratio for the variant design element comprises:

computing a yield and a change in area using the variant bit cell, wherein the yield is computed based on one or more existing failure models.

5. The method of claim 4, wherein the one or more existing failure models are obtained by:

extracting attributes from a product design layout;

designing failure model test chips based on the extracted attributes and possible modifications of the extracted attributes;

manufacturing the designed failure model test chips; and

testing and analyzing the manufactured failure model test chips to determine failures rates.

6. The method of claim 1, wherein the design element is a memory unit, the set of design elements is a set of memory units, and the variant design element is a redundancy unit, and further comprising:

sorting the memory units in the set of memory units in order of largest macro area to smallest macro area.

7. The method of claim 6, wherein determining a yield to area ratio for the variant design element comprises:

computing a yield and a change in area using the redundancy unit, wherein the yield is computed based on one or more existing failure models.

8. The method of claim 7, wherein the one or more existing failure models are obtained by:

extracting attributes from a product design layout;

designing failure model test chips based on the extracted attributes and possible modifications of the extracted attributes;

manufacturing the designed failure model test chips; and

testing and analyzing the manufactured failure model test chips to determine failures rates.

9. The method of claim 6, wherein the variant design element includes a bit cell modification.

10. The method of claim 1, wherein the design element is an embedded memory unit, the set of design elements is a set of embedded memory units, and the variant design element is a memory type, and further comprising:

sorting the memory units in the set of memory units in order of largest macro area to smallest macro area.

11. The method of claim 10, wherein determining a yield to area ratio for the variant design element comprises:

computing a yield and a change in area using a different memory type, wherein the yield is computed based on one or more existing failure models.

12. The method of claim 11, wherein the one or more existing failure models are obtained by:

extracting attributes from a product design layout;

designing failure model test chips based on the extracted attributes and possible modifications of the extracted attributes;

manufacturing the designed failure model test chips; and

testing and analyzing the manufactured failure model test chips to determine failures rates.

13. The method of claim 1, wherein the design element is a standard cell, the set of design elements is a library of standard cells, and the variant design element is a variant cell, and further comprising:

selecting one or more design modifications from a change list having a plurality of design modifications, wherein the feature of the standard is modified in accordance with the selected one or more design modifications.

14. The method of claim 13, further comprising:

compiling a usage listing of standard cells, wherein the usage listing is a pareto of the standard cells used most frequently in the design of the integrated circuit.

15. The method of claim 13, wherein the change list includes:

widening spacing between diffusions, polysilicon, or metal interconnections;

doubling contacts;

adding or widening borders on metal around contacts;

widening polysilicon interconnects; and

changing silicide overlaps.

16. The method of claim 13, wherein the one or more design modifications are selected based on existing failure models.

17. The method of claim 16, wherein the one or more existing failure models are obtained by:

extracting attributes from a product design layout;

designing failure model test chips based on the extracted attributes and possible modifications of the extracted attributes;

manufacturing the designed failure model test chips; and

testing and analyzing the manufactured failure model test chips to determine failures rates.

18. The method of claim 13, further comprising:

estimating an expected performance change for the variant cell; and

if the expected performance change is unacceptable, discarding the variant cell.

19. The method of claim 13, wherein the yield to area ratio determined for the variant design element is based on a layout generated based on potential corrective modifications.

20. The method of claim 19, wherein the plurality of design modification in the change list includes:

failure mechanisms and corresponding potential corrective modifications.

21. The method of claim 13, wherein a yield for the variant cell in an integrated circuit design is computed based on the number of occurrences of the variant cell in the integrated circuit design, and further comprising:

raising the yield of the variant in the yield to area ratio of the variant cell to the power of the number of occurrence of the standard cell in the integrated circuit design; and

raising the yield of the standard cell in the yield to area ratio of the standard cell to the power of the number of occurrence of the standard cell in the integrated circuit design.

22. The method of claim 13, further comprising:

identifying standard cells in the library to be modified using a selection criterion.

23. The method of claim 22, wherein the selection criterion is a measure or an estimate of maximum overall impact that modifications on a standard cell will have on the number of good dies per wafer (GDW) for a target product.

24. The method of claim 23, further comprising:

determining the GDW for the integrated circuit using the standard cells;

multiplying a resulting chip yield by the number of dies per wafer;

determining a different GDW for the integrated circuit that incorporates the variant cells;

multiplying the resulting chip yield by the number of die in a wafer;

determining a maximum increment of GDW for each standard cell by subtracting the difference of the GDW given by using the variant cell and the standard cell; and

sorting the standard cells by the maximum increment of GDW.

25. The method of claim 23, wherein the selection criterion includes:

a minimum increment GDW desired in the product;

a maximum number of standard cells to be modified; and

an incremental increase in GDW from modifying an additional standard cell.

26. The method of claim 1, wherein the design element is a gate-level net-list, the set of design elements is a set of gate-level net-lists, and the variant design element is a variant gate-level net-list, and wherein a feature of the obtained gate-level net-list is modified by:

changing a router/placer configuration file; or

changing router/placer/options switches.

27. The method of claim 13, further comprising:

selecting a set of figure of merit (FOM) circuits representative of types of designs to be implemented;

estimating a parametric yield of the FOM circuits using standard response surface methodology flows; and

determining a range or a set of values that make the FOM circuits achieve a desired parameter yield using yield impact graphs, wherein a yield impact graph plots a parametric yield as a function of process parameter distribution.

28. The method of claim 27, further comprising:

determining an estimate of robustness of a standard cell using a yield impact graph for the standard cell.

29. The method of claim 28, wherein the variant cell has a different performance, parametric yield, or robustness than the standard cell.

30. The method of claim 27, wherein a yield impact graph plot is generated by:

selecting a number of intervals for a mean of a set of electrical and physical parameters (m_i); and

running a simulation using a probabilistic model involving an element of chance on a space of means and standard deviations of uncorrelated parameters until:

a) for each interval of the mean of m_i, at least one distribution has a mean within the interval and a standard deviation less than a predetermined fraction of a standard deviation of m_i from a reference standard deviation of m_i; and

b) for each interval of the standard deviation of m_i, at least one distribution has a standard deviation within the interval and a mean less than a predetermined fraction of the mean of m_i from the reference mean of m_i.

31. The method of claim 30, wherein for each distribution that meets a),

running a simulation using a probabilistic model involving an element of chance, wherein at each interval a timing variable is computed and compared with timing specifications, wherein a minimum and maximum value of the timing variable is a model value of a minimum and maximum delay as a function of the means value of one m_i corresponding to a center of the interval of the mean of m_i, and wherein a ratio between the number of samples that meet a) and the total number of samples is a yield value of a speed-limited yield as a function of the mean value of one m_i.

32. The method of claim 30, wherein for each distribution that meets b),

running a simulation using a probabilistic model involving an element of chance, wherein at each interval a timing variable is computed and compared with timing specifications, wherein a minimum and maximum value of the timing variable is a model value of a minimum and maximum delay as a function of the standard deviation of one m_i corresponding to a center of the interval of the standard deviation of m_i, and wherein a ratio between the number of samples that meet b) and the total number of samples is a yield value of a speed-limited yield as a function of the standard deviation of one m_i.

33. The method of claim 30, wherein the simulation using a probabilistic model involving an element of chance is a Monte Carlo experiment, and wherein the predetermined fraction is 10 percent.

34. The method of claim 1, further comprising:

determining post tape-out modifications.

35. The method of claim 34, wherein determining post tape-out modifications comprises:

determining existing failures models;

determining modifications of layout attributes;

determining yield impact of the determined modifications;

generating a modified layout using the determined modifications;

predicting yield of the modified layout; and

verifying the modified layout.

36. The method of claim 35, wherein determining existing failure models comprises:

extracting attributes from a product design layout;

designing failure model test chips based on the extracted attributes and possible modifications of the extracted attributes;

manufacturing the designed failure model test chips; and

testing and analyzing the manufactured failure model test chips to determine failures rates.

37. A system for designing an integrated circuit to improve yield when manufacturing the integrated circuit, the system comprising:

a design element obtained from a set of design elements used in designing integrated circuits;

a variant design element created based on the obtained design element, wherein a feature of the obtained design element is modified to create the variant design element; and

a processor configured to:

determine a yield to area ratio for the variant design element, and

if the yield to area ratio of the variant design element is greater than a yield to area ratio of the obtained design element, retain the variant design element to be used in designing the integrated circuit.

38. The system of claim 37, further comprising:

one or more existing failure models, wherein the one or more existing failure models are obtained by:

extracting attributes from a product design layout;

designing failure model test chips based on the extracted attributes and possible modifications of the extracted attributes;

manufacturing the designed failure model test chips; and

testing and analyzing the manufactured failure model test chips to determine failures rates.

39. The system of claim 38, wherein the design element is a bit cell, the set of design elements is a set of bit cells, and the variant design element is a variant bit cell, and further comprising:

a selector configured to:

select a memory macro from a set of memory macros, and

apply the variant bit cell to the selected memory macro, wherein the variant bit cell is applied to each of the memory macros in order of size from smallest memory macro to largest memory macro.

40. The system of claim 39, wherein the yield to area ratio for the variant design element is determined by:

computing a yield and a change in area using the variant bit cell, wherein the yield is computed based on the one or more existing failure models.

41. The system of claim 38, wherein the design element is a memory unit, the set of design elements is a set of memory units, and the variant design element is a redundancy unit, and wherein the memory units in the set of memory units are sorted in order of largest macro area to smallest macro area.

42. The system of claim 41, wherein the yield to area ratio for the variant design element is determined by:

computing a yield and a change in area using the redundancy unit, wherein the yield is computed based on the one or more existing failure models.

43. The system of claim 41, wherein the variant design element includes a bit cell modification.

44. The system of claim 38, wherein the design element is an embedded memory unit, the set of design elements is a set of embedded memory units, and the variant design element is a memory type, and wherein the memory units in the set of memory units are sorted in order of largest macro area to smallest macro area.

45. The system of claim 44, wherein the yield to area ratio for the variant design element is determined by:

computing a yield and a change in area using a different memory type, wherein the yield is computed based the on one or more existing failure models.

46. The system of claim 38, wherein the design element is a standard cell, the set of design elements is a library of standard cells, and the variant design element is a variant cell, and further comprising:

a change list having a plurality of design modifications, wherein the feature of the standard is modified in accordance with the selected one or more design modifications.

47. The system of claim 46, further comprising:

a usage listing of standard cells, wherein the usage listing is a pareto of the standard cells used most frequently in the design of the integrated circuit.

48. The system of claim 47, wherein the change list includes:

widening spacing between diffusions, polysilicon, or metal interconnections;

doubling contacts;

adding or widening borders on metal around contacts;

widening polysilicon interconnects; and

changing silicide overlaps.

49. The system of claim 46, further comprising:

a selector configured to select one or more design modifications from the change list, wherein the one or more design modifications are selected based on the existing failure models.

50. The system of claim 46, wherein the processor is further configured to:

estimate an expected performance change for the variant cell; and

if the expected performance change is unacceptable, discard the variant cell.

51. The system of claim 46, wherein the yield to area ratio determined for the variant design element is based on a layout generated based on potential corrective modifications.

52. The system of claim 51, wherein the plurality of design modification in the change list includes:

failure mechanisms and corresponding potential corrective modifications.

53. The system of claim 46, wherein a yield for the variant cell in an integrated circuit design is computed based on the number of occurrences of the variant cell in the integrated circuit design, wherein the yield of the variant in the yield to area ratio of the variant cell is raised to the power of the number of occurrence of the standard cell in the integrated circuit design, and wherein the yield of the standard cell in the yield to area ratio of the standard cell is raised to the power of the number of occurrence of the standard cell in the integrated circuit design.

54. The system of claim 46, further comprising:

a selector configured to identify standard cells in the library to be modified using a selection criterion, wherein the selection criterion is a measure or an estimate of maximum overall impact that modifications on a standard cell will have on the number of good dies per wafer (GDW) for a target product.

55. The system of claim 54, wherein:

the GDW for the integrated circuit is determined using the standard cells;

a resulting chip yield is multiplied by the number of dies per wafer;

a different GDW for the integrated circuit is determined that incorporates the variant cells;

the resulting chip yield is multiplied by the number of die in a wafer;

a maximum increment of GDW for each standard cell is determined by subtracting the difference of the GDW given by using the variant cell and the standard cell; and

the standard cells are sorted by the maximum increment of GDW.

56. The system of claim 54, wherein the selection criterion includes:

a minimum increment GDW desired in the product;

a maximum number of standard cells to be modified; and

an incremental increase in GDW from modifying an additional standard cell.

57. The system of claim 38, wherein the design element is a gate-level net-list, the set of design elements is a set of gate-level net-lists, and the variant design element is a variant gate-level net-list, and wherein a feature of the obtained gate-level net-list is modified by:

changing a router/placer configuration file; or

changing router/placer/options switches.

58. The system of claim 46, further comprising:

a set of figure of merit (FOM) circuits representative of types of designs to be implemented, wherein a parametric yield of the FOM circuits is estimated using standard response surface methodology flows, and wherein a range or a set of values is determined that make the FOM circuits achieve a desired parameter yield using yield impact graphs, and wherein a yield impact graph plots a parametric yield as a function of process parameter distribution.

59. The system of claim 58, further comprising:

a yield impact graph for a standard cell, wherein an estimate of robustness of the standard cell is determined using the yield impact graph.

60. The system of claim 59, wherein the variant cell has a different performance, parametric yield, or robustness than the standard cell.

61. The system of claim 58, wherein a yield impact graph plot is generated by:

selecting a number of intervals for a mean of a set of electrical and physical parameters (m_i); and

running a simulation using a probabilistic model involving an element of chance on a space of means and standard deviations of uncorrelated parameters until:

a) for each interval of the mean of m_i, at least one distribution has a mean within the interval and a standard deviation less than a predetermined fraction of a standard deviation of m_i from a reference standard deviation of m_i; and

b) for each interval of the standard deviation of m_i, at least one distribution has a standard deviation within the interval and a mean less than a predetermined fraction of the mean of m_i from the reference mean of m_i.

62. The system of claim 61, wherein for each distribution that meets a),

running a simulation using a probabilistic model involving an element of chance, wherein at each interval a timing variable is computed and compared with timing specifications, wherein a minimum and maximum value of the timing variable is a model value of a minimum and maximum delay as a function of the means value of one m_i corresponding to a center of the interval of the mean of m_i, and wherein a ratio between the number of samples that meet a) and the total number of samples is a yield value of a speed-limited yield as a function of the mean value of one m_i.

63. The system of claim 61, wherein for each distribution that meets b),

running a simulation using a probabilistic model involving an element of chance, wherein at each interval a timing variable is computed and compared with timing specifications, wherein a minimum and maximum value of the timing variable is a model value of a minimum and maximum delay as a function of the standard deviation of one m_i corresponding to a center of the interval of the standard deviation of m_i, and wherein a ratio between the number of samples that meet b) and the total number of samples is a yield value of a speed-limited yield as a function of the standard deviation of one m_i.

64. The system of claim 61, wherein the simulation using a probabilistic model involving an element of chance is a Monte Carlo experiment, and wherein the predetermined fraction is 10 percent.

65. The system of claim 38, wherein the processor is further configured to determine post tape-out modifications.

66. The system of claim 65, wherein post tape-out modifications are determined by:

determining modifications of layout attributes;

determining yield impact of the determined modifications;

generating a modified layout using the determined modifications;

predicting yield of the modified layout; and

verifying the modified layout.

67. A computer readable storage medium containing computer executable instructions for causing a computer to aid in the design of an integrated circuit to improve yield when manufacturing the integrated circuit, comprising instructions for:

obtaining a design element from a set of design elements used in designing integrated circuits;

creating a variant design element based on the obtained design element, wherein a feature of the obtained design element is modified to create the variant design element;

determining a yield to area ratio for the variant design element; and

if the yield to area ratio of the variant design element is greater than a yield to area ratio of the obtained design element, retaining the variant design element to be used in designing the integrated circuit.